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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b))

Attorney Docket No. 94-0280.04		*Total Pages*	
First Named Inventor or Application Identifier			
Thomas A. Figura et al.			
Express Mail Label No.	EL003001606US		

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. ☒ Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. ☒ Specification *Total Pages* 20 *(preferred arrangement set forth below)*
   - -Descriptive
   - -Cross References to Related Application
   - -Statement Regarding Fed sponsored R & D
   - -Reference to Microfiche Appendix
   - -Background of the Invention
   - -Brief Summary of the Invention
   - -Brief Description of the Drawings *(if filed)*
   - -Detailed Description
   - -Claim(s)
   - -Abstract of the Disclosure
3. ☒ Drawing(s) *(35 USC 113)* *Total Sheets* 6 *Total Pages* 2
4. Oath or Declaration
   - a. ☐ Newly executed (original or copy)
   - b. ☒ Copy from a prior application (37CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
     - i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. ☐ Computer Readable Copy
   - b. ☐ Paper Copy (identical to computer copy)
   - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☒ 37 CFR 3.73(b) Statement ☒ Power of Attorney *(where there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
14. ☐ Small Entity ☐ Statement filed in prior application Statement(s) Status still proper and desired
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Other

17. ☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: ____/____

18. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* ☐ *Correspondence address below*

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Thomas A. Figura, Kevin Donohoe, & Thomas Dunbar	§	Group Art Unit:
Serial No.:	§	Application Examiner:
Filed: December 22, 1999	§	Atty. Docket: 94-0280.04
Title: USE OF A PLASMA SOURCE TO FORM A LAYER DURING THE FORMATION OF A SEMICONDUCTOR DEVICE	§	

PRELIMINARY AMENDMENT

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Signature

Assistant Commissioner for Patents

Washington, D.C. 20231

Dear Sir:

After awarding this application the benefit of the filing date of the great-grandparent application, filed June 2, 1995, please amend the accompanying continuation application as follows:

IN THE SPECIFICATION

After the title, please include the following --

RELATED APPLICATIONS

This application is a divisional of a pending U.S. application, serial number 09/046,835, filed on October 24, 1997; which is a continuation of U.S. application serial number 08/787,453, filed January 22, 1997 and issued on September 7, 1999 as U.S. Patent No. 5,950,092; which is a continuation of U.S. application Serial Number 08/458,861, filed June 2, 1995 and now abandoned. --

On page 6, line 2, please delete the second appearance of the word "generally".

Also on page 6, line 16, please replace "setting" with -- settings --.

In addition, on page 10, lines 5-7, please delete the sentence "Further, "polymer" is intended to describe any plasma-deposited material including (but not limited to) those materials comprising carbon and either or a halogen and/or hydrogen." and replace it with -- The plasma-deposited material can comprise polymers including (but not limited to) carbon and either a halogen and/or hydrogen or various other materials. --

Remarks

Claims 1-46 are pending. During prosecution of the parent application (serial number 09/046,835) the parent's Examiner issued a restriction requirement in the Office Action of October 20, 1998. Specifically, the Examiner indicated that the parent's claims were generic to three patentably distinct species as disclosed in Figures 1-4, 5-6, and 7-8, respectively. For purposes of examining this divisional application, Applicants request that the Examiner review the pending claims as they apply to the species disclosed in Figures 5-6. Please address further correspondence with this application to: Charles B. Brantley, II, Micron Technology, Inc., Mail Stop 525, 8000 S. Federal Way, Boise, ID 83706-9632, telephone number (208) 368-4557.

MICRON, TECHNOLOGY, INC.

Date 12/22/99

Charles Brantley

Charles B. Brantley II, Reg. No. 38,086

DOCKET NO.: 94-0280.04

APPLICATION FOR LETTERS PATENT

FOR

USE OF A PLASMA SOURCE TO FORM A LAYER DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

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USE OF A PLASMA SOURCE TO FORM A LAYER DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

Field of the Invention

The invention relates to the field of semiconductor manufacture, and more specifically to a method for forming and etching layers during the formation of a semiconductor device.

Background of the Invention

A typical structure formed during the manufacture of a semiconductor memory device is a container cell which requires several steps for its manufacture. A sample process for forming the container cell includes implanting a diffusion area in a semiconductor wafer substrate, and forming an insulator, such as borophosphosilicate glass (BPSG) or tetraethylorthosilicate (TEOS), over the wafer. The insulator is etched to open a contact, usually round or oval in shape, to expose the diffusion region. A compliant conductive layer such as doped polycrystalline silicon is formed over the wafer surface and within the contact which contacts the diffusion region. The conductive layer is masked to protect the portion within the contact and the remainder is etched. Various steps as known in the art are subsequently performed to produce a container cell.

The process described above requires the wafer to be transported between several chambers. The diffusion region is formed in an implanter, and the insulator, usually a blanket layer, is formed either in a furnace (to form TEOS) or in a chemical vapor deposition tool such as a Watkins-Johnson to form BPSG. Plasma-enhanced chemical vapor deposition (PECVD) and various other means can be used to form the insulator. The wafer is then moved to a stepper for patterning of the insulator, then to a dry etch chamber where the insulator is etched to form the contact. The wafer is moved again to a furnace, a low-pressure chemical vapor deposition (LPCVD) chamber, or a PECVD chamber to form a blanket conductive layer over the wafer surface and within the contact. Next, the conductive layer on the surface of the wafer is removed, for example using chemical mechanical planarization (CMP) equipment. The conductive layer can also be removed by forming a resist coat over the wafer, which forms a thicker layer within the contact than on the wafer surface, and dry etching the surface to remove the resist and poly from the surface while leaving a portion of the poly within the contact. Finally, the wafer is moved to an acid bath or a plasma etcher where the resist is stripped from the contact.

Transporting the wafer is not desirable as it increases processing time, costs, and possible damage and contamination to the wafer. A process which requires less wafer transportation is therefore desirable.

Summary of the Invention

A first embodiment of the invention is a method used during the formation of a semiconductor device comprising placing a semiconductor wafer having a surface and a recess formed in the wafer into a chamber of a plasma source. Within the chamber, a layer of etch resistant material is formed within the recess and over the surface of the wafer. Finally, also in the chamber, the etch resistant layer which forms over the surface of the wafer is removed and at least a portion of the etch resistant layer is left in the recess.

A second embodiment of the invention comprises a method used during the formation of a semiconductor device comprising placing a semiconductor wafer having a surface and a recess formed in the wafer into a chamber of a plasma source. Within the chamber, a layer of etch resistant material is formed within the recess, the etch resistant material not forming over the surface.

Objects and advantages will become apparent to those skilled in the art from the following detailed description read in conjunction with the appended claims and the drawings attached hereto.

Brief Description of the Drawings

FIGS. 1-4 are cross-sections of a first embodiment of the invention;

FIGS. 5-6 are cross-sections of a second embodiment of the invention; and

FIGS. 7-8 are cross-sections of a third embodiment of the invention.

It should be emphasized that the drawings herein are not to scale but are merely schematic representations and are not intended to portray the specific parameters or the structural details of the invention, which can be determined by one of skill in the art by examination of the information herein.

Detailed Description of the Invention

FIGS. 1-4 are cross-sections of a first embodiment of the invention used to form a storage node of a container cell. It should be noted that the invention can be used to form a number of other structures, and the use of the invention to form a storage node of a container cell is for ease of explanation.

A starting structure is shown in FIG. 1. The starting structure comprises a wafer 10 having a surface 12 and a contact 14 formed in the wafer. The wafer shown comprises a substrate 16, for example of silicon or gallium arsenide, and insulator 18, such as an

oxide or a nitride, with the contact formed in the insulator. The specific use of the invention shown further comprises a conductive layer 20 such as a conformal layer of polycrystalline silicon formed within the contact 14 and over the wafer surface 12 which contacts the substrate 16. The invention is described for a starting structure using a 1,000Å to 20,000Å thick BPSG layer as the insulator, a contact 0.2 to 1.0 microns in diameter, and a polycrystalline silicon conductor layer 200-2,000Å thick. Etcher settings listed below may require modification for different materials and/or thicknesses, which can easily be determined by one of ordinary skill in the art from the description herein without undue experimentation.

The structure of FIG. 1 is placed into a chamber of a plasma source such as a conventional plasma etcher or a high density plasma etcher. High density plasma etchers operate at pressures below 50 millitorr (typically below 10 millitorr) and have plasma densities greater than 10^{10} to 10^{11} cm^{-3}. In addition, most etch applications of high density plasma etchers use two sources of electrical power, one to generate the plasma and one to bias the wafer. The plasma source can be an etcher such as an Applied Materials Model 5300 HDP, LAM TCP, or other such etcher. A layer of etch resistant material 22, such as a polymer, is formed within the contact 14 and over the surface 12 of the wafer 10 as shown in FIG. 2. The etch resistant material bridges across the contact and fills in the contact. In general, any feed gas which forms an etch resistant layer can be used. For example, fluorocarbons, hydrofluorocarbons, chlorofluorocarbons, halocarbons or hydrohalocarbons would function sufficiently. Examples include CHF_3, CH_2F_2, C_2F_6, C_2HF_5, C_3F_8. The flow rate depends on which feed gas is used, and can be determined by one of skill in the art

from the description herein without undue experimentation. Generally, flow rates would generally be in the range of 25-200 standard cubic centimeters (sccm) although flow rates outside this range may function adequately. To bridge over a contact 0.5 microns in diameter and form a polymer layer about 2000 angstroms (Å) thick over the wafer surface, the following settings can be used:

Source (top) Power:	From 1000 to 3500 Watts
Bias (bottom) Power:	From 0 to 400 Watts
Pressure:	From 2 to 5 Millitorr
Duration:	From 5 to 40 Seconds
Flow Rate:	From 10 to 50 SCCM

These settings usually cause the etch resistant layer formed on the surface to be thinner than the material formed within the contact. It should be noted that there is an interaction between the listed parameters, and other settings in addition to the ranges listed above may also function adequately. The setting herein can be altered by one of ordinary skill in the art from the description herein to customize the etch resistant layer formation for various sizes and shapes of contact, and for various thicknesses within the contact and over the wafer surface. Depending on the application, any thickness of etch-resistant layer may be useful, but an etch-resistant layer 50Å or greater is preferred for most applications.

Next, within the chamber, the etch resistant layer is removed from the wafer surface as shown in FIG. 3 using parameters known in the art. Because the etch resistant layer bridges across the contact, and essentially forms a thicker layer within the contact, the layer can be removed from the surface while at least a portion 30 of the layer remains

within the contact as shown in FIG. 3. In addition, the portion of the conductive layer 20 on the wafer surface 12 can also be removed using the same settings used to remove the etch resistant layer from the wafer surface, or different settings can be used depending on the material of layer 20. The remaining portion of the etch resistant layer 30 functions as a mask to protect the conductive layer 32 within the contact.

The etch resistant layer 30 can be removed, for example within the chamber, to expose the conductive layer 32 to result in the structure of FIG. 4. The etch resistant layer 30 can be removed using etcher settings similar to those used for stripping photoresist. Oxygen-fluorocarbon mixtures are best suited for this since layer 30 may comprise some silicon. Using subsequent processing steps element 32 can function as a capacitor storage node, although there are many other uses for the inventive method. Removal of insulator 18 can be accomplished with any means, such as within the etch chamber or outside the chamber, for example in a hydrofluoric acid (HF) sink.

A second embodiment of the invention is shown in FIGS. 5 and 6. The starting structure of FIG. 1 is placed into a chamber of a plasma source. Using a combination of etcher settings, an etch resistant layer 50 can be formed within the contact 14, or other narrow openings, without the etch resistant layer forming on the wafer surface 12 to result in the structure of FIG. 5. The thickness of the etch resistant layer which forms within the contact is dependent on the duration of the step. As the layer thickens its rate of formation slows and may eventually stop. Forming the etch resistant layer in the contact and not on the wafer surface results in part from operating at a higher bias voltage and under conditions of

lower deposition rate than in the first embodiment. For example, in the Applied Materials HDP Etch tool, these conditions would include lowering the source power and decreasing the total flow rate of process gasses. The specific values of the operating parameters can be adjusted by one of skill in the art from the information herein.

The etch resistant layer can then be used as a mask and the conductive layer 20 can be etched with a separate etch step, for example in the same etch chamber, according to means known in the art. Next, the etch resistant layer 50 can be removed as described with the first embodiment above to result in the structure of FIG. 4.

A third embodiment of the invention is shown in FIGS. 7-8. The starting structure of FIG. 7 is placed in an etch chamber. By decreasing the deposition rate and increasing the bias of the settings shown for the first embodiment, an etch resistant layer 80 can be formed within the contact 14 while, simultaneously, the conductive layer 20 is etched from the surface of the wafer. As the polymer builds up over the conductive layer 20 within the contact 14, it functions as a mask and protects the horizontal surface of the conductive layer in the contact. The conductive layer is simultaneously removed from the surface of the wafer. Some attack on the top of 20 may occur with this embodiment, but such an attack does not affect the performance of the container cell.

The inventive method as described in the embodiments above has the advantage of forming a mask in an etch chamber. Subsequent etches can also be performed within the chamber. Performing a number of different steps within the etch chamber decreases

the transportation requirements of the wafer which reduces production time and decreases damage resulting from handling of the wafers.

The three embodiments described have various deposition rates of the polymer on the wafer surface compared with the deposition rate of the polymer within the recess. With the first embodiment, the polymer forms faster within the recess than on the wafer surface. In the second embodiment, the polymer does not form on the wafer surface but forms within the recess. In the third embodiment, an etch occurs on the wafer surface while the polymer forms within the recess. The deposition rate of the polymer on the wafer surface can be decreased as compared to the polymer formation within the recess by various means, such as by decreasing the source power, by decreasing the flow rate, by increasing the bias power, or by using a combination of these parameters. Other methods of controlling the deposition rate may also be possible and apparent to one of skill in the art from reviewing the information herein. These other methods fall within the scope of the invention.

While this invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. For example, the etch resistant layer can be formed within any recess such as a trench, via, contact, depression in an exposed surface with modifications to the etcher settings. Depending on the size of the recess, the etcher settings may require modification, which

can be determined without undue experimentation from the disclosure herein. Also, the recess can be formed in an oxide layer as shown herein, or can be formed within the wafer substrate, between two protruding features, or in other layers. The term "wafer assembly" is used to describe a raw substrate, a substrate with doped regions therein, or a substrate with a layer or layers such as oxide or nitride thereon. Further, "polymer" is intended to describe any plasma-deposited material, including (but not limited to) those materials comprising carbon and either or a halogen and/or hydrogen. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

Claims

What is claimed is:

1. A method of forming a semiconductor device, comprising:

providing a surface within said semiconductor device;

providing a first feature on said surface;

providing a second feature on said surface; and

forming a polymer between said first feature and said second feature in a high-density plasma environment.

2. The method in claim 1, further comprising modifying said polymer within said high-density plasma environment.

3. The method in claim 2, wherein said step of modifying said polymer further comprises etching a portion of said polymer.

4. The method in claim 3, wherein said step of providing a first feature further comprises providing a first metallic feature; and providing a second feature further comprises providing a second metallic feature.

5. The method in claim 4, wherein said step of providing a first feature further comprises providing a first feature made of a metal; and providing a second feature further comprises providing a second feature made of said metal.

6. The method in claim 5, wherein said step of providing a first feature further comprises providing a first metal line; and providing a second feature further comprises providing a second metal line.

7. A method of processing a semiconductor device, comprising:

providing a first protruding feature on a layer of said semiconductor device;

providing a second protruding feature on said layer;

defining a recess between said first protruding feature and said second protruding feature; and

plasma-depositing a material within said recess.

8. The method in claim 7, wherein said step of plasma-depositing a material further comprises plasma-depositing a material comprising carbon and a halogen.

9. The method in claim 8, wherein said step of plasma-depositing a material further comprises plasma-depositing a hydrogen-free material.

10. The method in claim 7, wherein said step of plasma-depositing a material further comprises plasma-depositing a material comprising carbon and hydrogen.

11. The method in claim 10, wherein said step of plasma-depositing a material further comprises plasma-depositing a halogen-free material.

12. The method in claim 7, wherein said step of plasma-depositing a material further comprises depositing a material comprising carbon, a halogen, and hydrogen.

13. A method of depositing a polymer onto a wafer, comprising:

defining an opening between exposed metal protruding features on said wafer;

providing a plasma; and

exposing said opening to said plasma.

14. The method in claim 13, wherein said step of providing said plasma further comprises providing a high-density plasma.

15. The method in claim 14, wherein said step of providing a high-density plasma further comprises providing a plasma having a density higher than $10^{10}/cm^3$.

16. The method in claim 15 wherein said step of providing a high-density plasma further comprises providing a plasma having a density higher than $10^{11}/cm^3$.

17. The method in claim 16, wherein said step of providing a plasma further comprises providing a plasma comprising a selection from fluorocarbons and hydrofluorocarbons.

18. The method in claim 17, wherein said step of providing a plasma further comprises providing a plasma comprising a selection from C_2F_6 and CHF_3.

19. A method of providing a polymer between metal lines on a wafer, comprising:
providing a plasma source;
exposing said wafer to said plasma source;
introducing a feed gas to said wafer;
establishing a pressure around said wafer; and
forming said polymer between said metal lines using said feed gas.

20. The method in claim 19, wherein said step of providing a plasma source further comprises providing a plasma source chamber; and exposing said wafer to said plasma source further comprises placing said wafer in said plasma source chamber.

21. The method in claim 20, wherein said step of providing a plasma source further comprises providing an etching machine.

22. The method in claim 21, wherein said step of providing an etching machine further comprises providing a high-density plasma etching machine.

23. A method of forming a polymer, comprising:

providing a semiconductor device having at least two exposed metal lines; and

performing a process on said semiconductor device, wherein said process is defined by a plurality of parameters, comprising:

a source power magnitude,

a bias power magnitude,

a pressure,

a duration, and

a process gas flow rate.

24. The method in claim 23, wherein said step of performing said process further comprises:

providing a high-density plasma etcher having a plurality of process settings, comprising:

a source power setting,

a bias power setting,

a pressure setting,

a duration setting, and

a process gas flow rate setting; and

placing said semiconductor device in said etcher.

25. The method in claim 24, further comprising:

defining a recess between said exposed metal lines;

filling said recess with said polymer; and

allowing a formation of said polymer above said exposed metal lines.

26. The method of claim 25, wherein said step of allowing a formation of polymer above said exposed metal lines further comprises interactively establishing said plurality of process settings.

27. The method in claim 26, further comprising removing any of said polymer above said exposed metal lines.

28. The method in claim 27, further comprising removing said polymer while said semiconductor device is within said high-density plasma etcher.

29. A method of selectively forming a polymer, comprising:

providing a semiconductor device having a plurality of exposed protruding features;

providing an etcher having high-density plasma process settings, comprising:

a source power setting,

a bias power setting, and

a flow rate setting; and

exposing said semiconductor device to a high-density plasma process within said etcher.

30. The method in claim 29, further comprising:

defining at least one recess with said plurality of exposed protruding features;

filling said recess with said polymer; and

restricting formation of said polymer to within said recess.

31. The method in claim 30, wherein said step of defining at least one recess with said plurality of exposed protruding features comprises defining a recess between two protruding features of said plurality of protruding features.

32. The method in claim 31, wherein said step of restricting formation of said polymer to within said recess further comprises preventing a formation of said polymer above said two protruding features.

33. The method in claim 32, wherein said step of preventing a formation of said polymer above said two protruding features further comprises establishing said plasma process settings, wherein said plasma process settings interactively define a plurality of overflow parameters that allow formation of said polymer above said two protruding features, and wherein establishing said plasma process settings further comprises initiating at least one setting from a selection of settings comprising:

a source power setting lower than a source power setting that partially defines one of said overflow parameters;

a bias power setting higher than a bias power setting that partially defines one of said overflow parameters; and

a flow rate setting lower than a flow rate setting that partially defines one of said overflow parameters.

34. The method in claim 32, wherein said step of preventing a formation of said polymer above said two protruding features further comprises initiating a bias power setting generally greater that 0 watts.

35. The method in claim 34, wherein said step of providing a semiconductor device further comprises providing an in-process semiconductor device.

36. A method of selectively providing a material between two metal lines of a semiconductor device, comprising:

forming said material on said semiconductor device in a deposition environment; and

removing any excess of said material in an etching environment, wherein said etching environment is the same as said deposition environment.

37. The method in claim 36, wherein said step of forming said material further comprises forming said material in an etch chamber.

38. The method in claim 36, wherein said step of removing any excess of said material further comprises removing any excess of said material in a plasma deposition chamber.

39. A method of processing a wafer having metal lines, comprising:

providing a high-density plasma; and

forming a polymer between said metal lines using said high-density plasma.

40. A method of developing an in-process semiconductor device having a first metal line and a second metal line, comprising:

placing said device in a deposition and etch surrounding; and

forming a polymer between said first metal line and said second metal line.

41. The method in claim 40, further comprising:

providing a layer over said polymer; and

retaining a state of said polymer.

42. The method in claim 41, wherein said step of retaining said state of said polymer further comprises having a polymer with a thermal stability sufficient to withstand providing said layer.

43. The method in claim 42, wherein said step of providing said layer further comprises providing said layer outside of said deposition and etch surrounding.

44. A method of providing a polymer between metal features on a wafer, comprising:

performing a deposition on said wafer in a site; and

etching said wafer in the same general site used to perform said deposition.

45. The method in claim 44, wherein said step of etching said wafer further comprises etching said wafer generally simultaneously with performing said deposition.

46. The method in claim 45, wherein said step of performing a deposition further comprises depositing said polymer on said wafer.

ABSTRACT

A method used to form a semiconductor device having a capacitor comprises placing a semiconductor wafer assembly into a chamber of a plasma source, the wafer assembly comprising a layer of insulation having at least one contact therein and a surface, and further comprising a conductive layer over the surface and in the contact. Next, in the chamber, a layer of etch resistant material is formed within the contact over the conductive layer, the etch resistant material not forming over the surface.

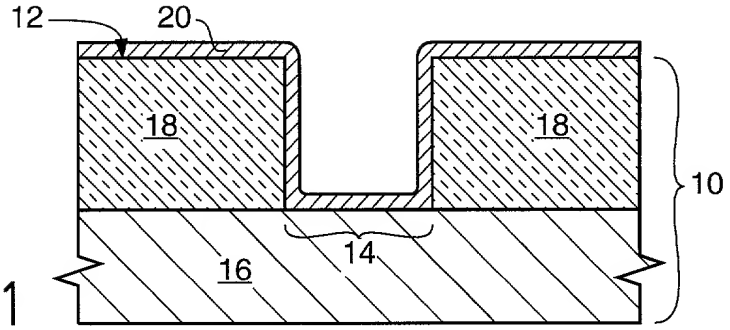

FIG. 1

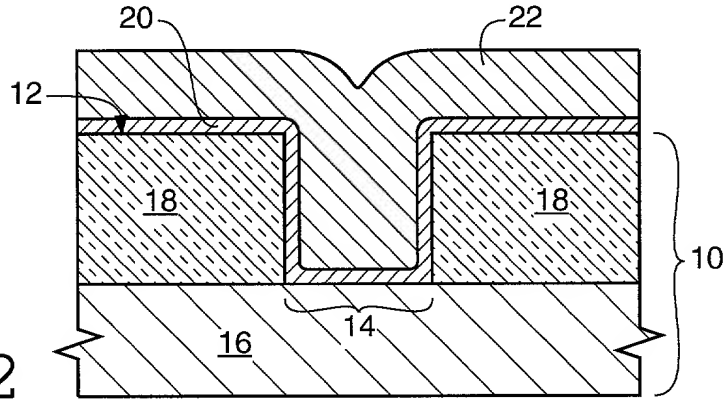

FIG. 2

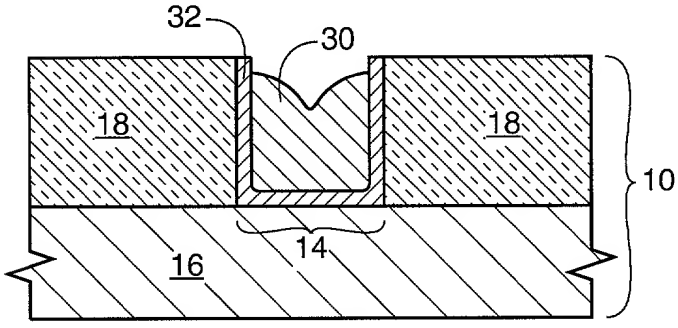

FIG. 3

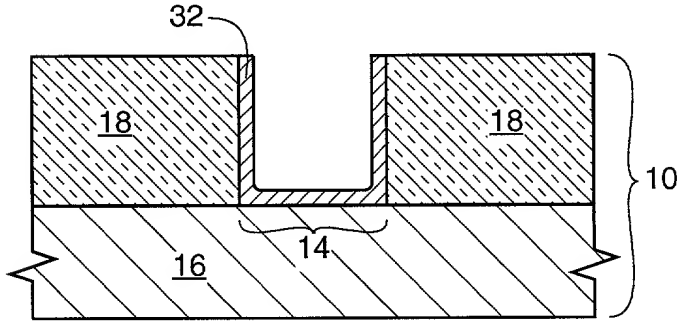

FIG. 4

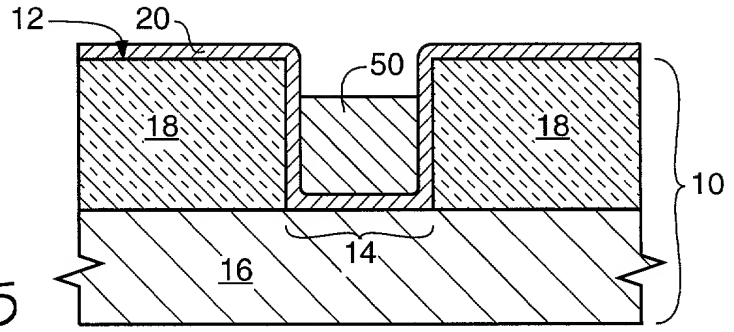

FIG. 5

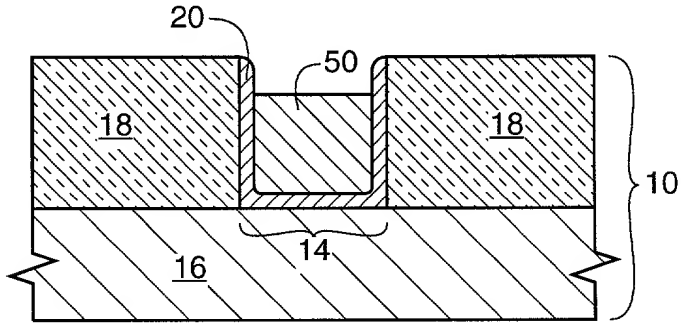

FIG. 6

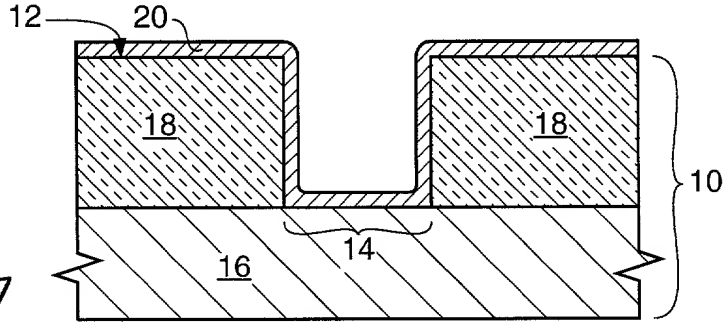

FIG. 7

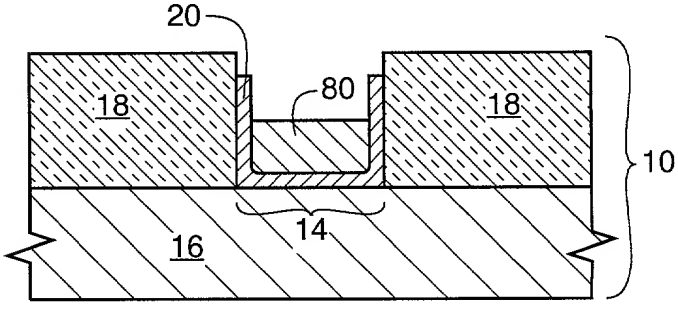

FIG. 8

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "USE OF A PLASMA SOURCE TO FORM A LAYER DURING THE FORMATION OF A SEMICONDCUTOR DEVICE", the specification of which:

X is attached hereto.

X was filed on January 22, 1997, as Application Serial No. 08/787,453, which, in turn, is a continuation of U. S. Application Serial No. 08/458,861, filed June 2, 1995.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability of the subject matter claimed in this application as "materiality" is defined in Title 37 of the Code of Federal Regulations, § 1.56.

I hereby claim the benefit of any earlier filing date in the United States to which I am entitled under Title 35 of the United States Code, § 120 and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 of the United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

08/458,861	June 2, 1995	Abandoned
(Application Serial No.)	(Filing Date)	(Status)

Send correspondence to:

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Mail Stop 525
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Boise, Idaho 83706
(208) 368-4557

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first or sole inventor: Thomas A. Figura

Inventor's Signature: Thomas A. Figura
(First, Middle Initial, Last)

Date: 23-OCT-1997

Residence Address: 5745 Elkhorn Avenue

City, State, Country: Boise, Idaho 83705 United States of America

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Full name of first or sole inventor: Kevin G. Donohoe

Inventor's Signature: Kevin G Donohoe
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Date:

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Full name of first or sole inventor: Thomas Dunbar

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Date:

Residence Address: ~~1101 Fairview Avenue~~ 3850 W. Adobe Ct. Tr.

City, State, Country: Boise, Idaho ~~83713~~ 83705 United States of America

Citizenship: United States of America

Post Office Address: Same as residence address

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Thomas A. Figura, Kevin G. Donohoe, and Thomas Dunbar

Serial No.:

Filed: December 22, 1999

For: USE OF A PLASMA SOURCE TO FORM A LAYER DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

§ Atty. Docket: 94-0280.04

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I HEREBY CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 C.F.R § 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Signature

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment recorded in the United States Patent and Trademark Office as set forth below or filed herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor(s).

The Assignee hereby revokes any previous Powers of Attorney and appoints: Charles B. Brantley, II, Reg. No. 38,086; Michael L. Lynch, Reg. No. 30,871; Lia M. Pappas, Reg. No. 34,095; Walter D. Fields, Reg. No. 37,130; Kevin D. Martin, Reg. No. 37,882; and David J. Paul, Reg. No. 34,692 as its attorney or agent, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., referenced below, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Assignment:

____Filed concurrently herewith for recording, a copy of which is attached hereto.

_X_ Previously recorded on: 10/24/97, at Reel: 9249, Frame: 0513.

Please direct all communications as follows:

Charles B. Brantley, Mail Stop 525
MICRON TECHNOLOGY, INC.
8000 S. Federal Way
Boise, ID 83716-9632
(208) 368-4557

ASSIGNEE: MICRON TECHNOLOGY, INC.

Date: Dec 22, 1999

By:
Michael L. Lynch, Reg. No. 30,871
Chief Patent Counsel

United States Patent & Trademark Office

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